

AMENDMENTS TO THE CLAIMS

Please **CANCEL** claims 22-24 without prejudice or disclaimer.

Please **ADD** claims 46-57 as shown below.

The following is a complete list of all claims in this application.

1-45. (Cancelled)

46. (New) A thin film transistor (TFT) array panel, comprising:

a substrate;

a gate wire formed on the substrate and including a gate line, a gate electrode and a gate pad and;

a gate insulating layer pattern formed on the gate wire and having a contact hole exposing the gate pad;

a semiconductor layer pattern formed on the gate insulating layer pattern;

an ohmic contact layer pattern formed on the semiconductor layer pattern;

a data wire formed on the ohmic contact layer pattern, including a data line, a source electrode, a drain electrode and a data pad, and having a boundary line substantially the same as that of the ohmic contact layer pattern;

a passivation layer pattern formed on the data wire, having contact holes exposing the gate pad, the data pad and the drain electrode; and

a pixel electrode electrically connected to the exposed portion of the drain electrode,

wherein the gate insulating layer pattern is formed along with at least one of the semiconductor pattern, the ohmic contact layer pattern, the data wire, the passivation layer pattern and the pixel electrode through a single photolithography process using a photoresist pattern having more than two different thickness that varies depending on positions.

47. (New) The TFT array panel of claim 46, further comprising a storage electrode formed over the gate line, wherein the semiconductor layer pattern and the ohmic contact layer pattern have a portion interposed between the storage electrode and the gate line, and the storage electrode is connected to the pixel electrode.

48. (New) The TFT array panel of claim 46, wherein the passivation layer pattern has a boundary line substantially the same as that of the semiconductor layer pattern except for portions adjoining the drain electrode and the data pad, having a width greater than that of the data wire, and covering a boundary line of the data wire;

49. (New) The TFT array panel of claim 46, wherein a portion of the pixel electrode is in direct contact with the gate insulating layer pattern.

50. (New) The TFT array panel of claim 46, wherein the gate insulating layer pattern has a shape different from that of the passivation layer pattern under the pixel electrode.

51. (New) The TFT array panel of claim 46, further comprising a redundant gate pad and a redundant data pad covering the gate pad and the data pad, respectively.

52. (New) A thin film transistor (TFT) array panel, comprising:

- a substrate;
- a gate wire formed on the substrate and including a gate line, a gate electrode and a gate pad;
- a gate insulating layer pattern formed on the gate wire and having a contact hole exposing the gate pad;
- a semiconductor layer pattern formed on the gate insulating layer pattern;
- an ohmic contact layer pattern formed on the semiconductor layer pattern;
- a data wire formed on the ohmic contact layer pattern, including a data line, a source electrode, a drain electrode and a data pad, and having a planar shape substantially the same as that of the ohmic contact layer pattern due to simultaneous etching;
- a passivation layer pattern formed on the data wire, having contact holes exposing the gate pad, the data pad and the drain electrode; and
- a pixel electrode electrically connected to the exposed portion of the drain electrode.

53. (New) The TFT array panel of claim 52, further comprising a storage electrode formed over the gate line, wherein the semiconductor layer pattern and the ohmic contact layer pattern have a portion interposed between the storage electrode and the gate line, and the storage electrode is connected to the pixel electrode.

54. (New) The TFT array panel of claim 52, wherein the passivation layer pattern has a boundary line substantially the same as that of the semiconductor layer pattern except for

portions adjoining the drain electrode and the data pad, having a width greater than that of the data wire, and covering a boundary line of the data wire.

55. (New) The TFT array panel of claim 52, wherein a portion of the pixel electrode is in direct contact with the gate insulating layer pattern.

56. (New) The TFT array panel of claim 52, wherein the gate insulating layer pattern has a shape different from that of the passivation layer pattern under the pixel electrode.

57. (New) The TFT array panel of claim 52, further comprising a redundant gate pad and a redundant data pad covering the gate pad and the data pad, respectively.